

In the Specification:

Pages 25-26, Paragraph 61, kindly amend as follows:

[0061] The data to be encoded is transferred to data input register 34. Data input register 34 is a parallel-in serial-out register. Data input register 34 is loaded with n bits of data, n being the number of bit positions that may be encoded into a half cycle of the sinusoidal carrier. Data input register 34 is falling-edge clocked by the data output of non-volatile memory 32. Prior to the first clock pulse, the first data bit appears at the serial output of data input register 34. When the output count of 9-bit counter 22 reaches the value corresponding to the phase angle location of the first data bit to be encoded, the output of non-volatile memory 30 presents a “1” value as previously disclosed. If the value of the first data bit appearing at the serial output of data input register 34 is also a “1” value, the output of AND gate 36 becomes true (a value of “1”). This latches the count of 9-bit counter 22 at the output of latch ~~24~~26, causing the output of D/A converter 30 to remain constant. From an examination of FIG. 3, persons of ordinary skill in the art will appreciate that delay element 24 is interposed in the output path of counter 22 to allow the output of nonvolatile memory 32 and the output of AND gate 36 to settle prior to the new count reaching latch 26.

Page 30, Paragraph 71, kindly amend as follows:

[0071] FIG. 4A is a block diagram of a frequency up converter that may be used for preparing modulated carriers for transmission in communications systems according to the present invention. Local oscillator 40 drives one input of balanced RF mixer 42. A modulated sinewave carrier set is presented to the other input of balanced RF mixer ~~40~~42. The output of balanced RF mixer ~~40~~42 is passed through bandpass filter 44. The arrangement of FIG. 4A for use as an upconverter is well known in the RF art.

Pages 30-31, Paragraph 72, kindly amend as follows:

[0072] FIG. 4B is a block diagram of a frequency down converter that may be used for downconverting received modulated carrier signals in communications systems according to the present invention. As in FIG. 4A, local oscillator 40 drives one input of balanced RF mixer 42. The received RF input presented to the other input of balanced RF mixer ~~40-42~~ through bandpass filter 46. The output of balanced RF mixer ~~40-42~~ is passed to a detector of the type disclosed herein. The arrangement of FIG. 4B for use as a downconverter is also well known in the RF art.

Page 37, Paragraph 86, kindly amend as follows:

[0086] The outputs of the LUTs 68-1 through 68-6 are presented to D/A converters 70-1 through 70-6, respectively. The D/A converters 70-1 through 70-6 linearly and continuously convert the parallel 8-bit digital byte from the LUTs 68-1 through 68-6 to the input of the summing amplifier 72. The summing amplifier 72 is a conventional configuration of a circuit using an operational amplifier to linearly add several individual analog signals together to produce one composite signal.

Page 39, Paragraph 90, kindly amend as follows:

[0090] In a communications system according to the present invention that employs a plurality of modulated carriers within a communications channel, provision is made for separately demodulating each of the carriers to extract the encoded data. Referring now to FIG. 7, a block diagram shows an input line 90 driving a plurality of illustrative balanced mixers 92, 94, 96, 98, ~~80, and 82-100, and 102~~. Six balanced mixers are shown in FIG. 7, but persons of ordinary skill in the art will readily understand that any number of balanced mixers could be used depending on how many

different-frequency modulated sinewaves were generated by the modulator circuitry of FIG. 5A.

Page 51, Paragraph 116, kindly amend as follows:

[0116] Referring now to FIG. 14, a FFT DSP embodiment of a demodulator circuit according to the present invention is disclosed. FFT technologies are well known in the art. The demodulator circuit comprises A/D converter 216 and FFT block 218.

Pages 52-53, Paragraph 120, kindly amend as follows:

[0120] The microcontroller 228 also commands and controls the interface to the IFFT and FFT blocks 232 and 234. The microcontroller ~~234~~228 receives the data from the 10/100 and USB bus 230 and formats it to the appropriate output to the IFFT 232 to generate the necessary signals for outputting to the phone line. The microcontroller 228 also receives digital words from the FFT block 234 and interprets these digital words for data content before passing them on to 10/100 and USB bus 230. The system clock for microcontroller is provided by the timing generator 236. The timing generator 236 provides clocks and system synchronization for system operation

Pages 53-54, Paragraph 122, kindly amend as follows:

[0121] The 16-bit D/A converter 238 linearly and continuously converts the parallel 16-bit digital word from the output of the Inverse Fast Fourier Transform (IFFT) ~~234~~232 block to a representative analog level. The continuous sequential stream of analog output samples produce, over time, a composite output analog signal which is fed through the switch ~~204~~224 and the hybrid ~~202~~222 to the phone line. The sample rate for constructing the analog signal is determined by the timing generator 236.

Page 54, Paragraph 123, kindly amend as follows:

[0123] A 16 bit A/D block 240 linearly converts the analog output from the hybrid ~~202~~222 through the switch ~~204~~224 to 16-bit digital words which are representations of each sampled analog level. The 16-bit samples are fed in parallel to the input of the Fast Fourier Transform (FFT) 234. The sample rate of the analog signals to the digital words is determined by the timing generator 236.

Page 54, Paragraph 124, kindly amend as follows:

[0124] The Fourier Transform (FFT) 234 is a digital signal processing (DSP) process that converts analog signals in the time domain to a digital representation of the signal in the frequency domain. Digital words representing time domain samples from the A/D converter 240 are fed in parallel to the FFT 234. The FFT 234 subsequently outputs to the microcontroller ~~208~~228, parallel digital word(s) which are representative of the frequency components of the sampled time domain (analog) signal. The conversion clock and synchronization of the FFT conversion is provided by the timing generator ~~238~~236.

Page 54, Paragraph 125, kindly amend as follows:

[0125] The system 200 negotiates a connection using the V.90 modem. If the other station indicates that it can communicate using the techniques of the present invention, the microcontroller ~~208~~228 causes switch ~~204~~224 to connect the D/A converter 238 and the A/D converter 240 to the hybrid 222 instead of the V.90 modem.

Pages 55-56, Paragraph 128, kindly amend as follows:

[0128] A double balanced mixer ~~268~~258 mixes the incoming signal with the output of a local oscillator producing the sum and difference of the two signals. The local oscillator may be formed from a zero crossing detector 260 that produces an output when the incoming signal crosses the zero-volt level. The zero crossing detector 260 is used to generate the reference for the carrier regenerator 262 that acts as the local oscillator and the phase lock loop 264 which generates the data clock. The carrier regenerator takes the output of the zero crossing detector and creates a local oscillator output which is the same frequency and phase of that of the incoming signal. Phase locked loop 264 uses the output of the zero crossing detector 260 to generate a high frequency clock used to clock the retrieved data at the output of the comparator 268.

Page 56, Paragraph 129, kindly amend as follows:

[0129] Low pass filter 266 removes the sum frequency component from the output of the mixer 258, leaving the difference component which is representative of the absolute phase difference between the input signal and the reference signal out of the local oscillator. Comparator 268 compares the difference signal from the mixer 258 to a fixed reference producing an output when the input signal is higher than the reference signal. An output indicates there is a phase difference between input and local oscillator indicating the presence of a data bit of value "one".

Page 56, Paragraph 130, kindly amend as follows:

[0130] Clock alignment block 270 under the control of the microcontroller 272 aligns the data clock through a variable delay circuit. Using ~~apriori~~ a prior knowledge of where in the phase of the signal where the data bits are this circuit filters out data clock

pulses which are not in alignment with known valid data bits coming out of the comparator. The data is clocked into the multi-stage shift register 274 that is used as a gathering repository for the data bits clocked in from the output of the comparator 268. Microcontroller 272 is a preprogrammed device which monitors and controls the operation of the receiver. Microcontroller 272 transfers the received data stored in the shift register out to other areas.